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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,787	02/25/2002	Rajendra Pendse	CPAC 1010-2 US	6217

22470 7590 06/11/2003

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EXAMINER
WILLIAMS, ALEXANDER O

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/084,787	Applicant(s) PENDSE ET AL.	
	Examiner Alexander O Williams	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Serial Number: 10/084787 Attorney's Docket #: CPAC 1010-2US
Filing Date: 2/25/02; priority to 2/27/01

Applicant: Pendse et al.

Examiner: Alexander Williams

Applicant's Amendment in Paper # 6, filed 12/9/02 has been acknowledged.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 to 4 and 6 to 8 are rejected under 35 U.S.C. § 102(b) as being anticipated by David et al. (Japan Patent # 2000-156457).

For example, in claim 1, David et al. (figures 1 to 3) specifically **figure 3** show a chip scale integrated circuit chip package comprising a die **10** mounted by flip chip interconnection to a first surface of a package substrate **14**, wherein the flip chip interconnection comprises solid state connections **(see the abtract's solution section)** of interconnect bumps **18** affixed to the die with interconnect pads **12** on the first surface of the substrate, and second level interconnections **16** formed on the first surface of the package substrate.

Claims 1 to 4 and 6 to 8 are rejected under 35 U.S.C. § 102(b) as being anticipated by Maeta et al. (U.S. Patent # 5,677,246).

For example, in claim 1, Maeta et al. (figures 1B to 18B) specifically **figure 11** show a chip scale integrated circuit chip package comprising a die **2** mounted by flip chip interconnection to a first surface of a package substrate **1**, wherein the flip chip interconnection comprises solid state connections **(see column 12, lines 45-53)** of interconnect bumps **1b** affixed to the die with interconnect pads **2a** on the first surface of the substrate, and second level interconnections **1a** formed on the first surface of the package substrate.

Claims 1 to 4, 6 to 9 and 11 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Rolda, Jr. et al. (U.S. Patent Application Publication # 2002/0030261 A1) in view of David et al. (Japan Patent # 2000-156457).

For example, in claim 1, Rolda, Jr. et al. (figures 1 and 2) specifically figure 1 show a chip scale integrated circuit chip package **100** comprising a die **130** mounted by flip chip interconnection to a first surface **122** of a package substrate **120**, wherein the flip chip interconnection comprises solid state connections of interconnect bumps affixed to the die with interconnect pads on the first surface of the substrate, and second level interconnections **161** formed on the first surface of the package substrate. Rolda, Jr. et al. fail to explicitly show the flip chip interconnection comprises solid state connections of interconnection bumps affixed to the die with interconnection pads on the first surface of the substrate. However, Rolda, Jr. et al. does discloses the structures claimed of the chip, substrate and pads connected. It would be obvious to one of ordinary skill in the art to use solid state connection as a design choice.

David et al. is cited for showing a semiconductor device. Specifically, David et al. (figures 1 to 3) specifically **figure 3** show a chip scale integrated circuit chip package comprising a die **10** mounted by flip chip interconnection to a first surface of a package substrate **14**, wherein the flip chip interconnection comprises solid state connections **(see the abtract's solution section)** of interconnect bumps **18** affixed to the die with interconnect pads **12** on the first surface of the substrate, and second level interconnections **16** formed on the first surface of the package substrate for the purpose of providing a interconnection of an integrated circuit chip and a board of a multi-chip module.

Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to use David et al.'s solid state connection to modify Rolda, Jr. et al.'s connection for the purpose of providing a interconnection of an integrated circuit chip and a board of a multi-chip module.

Claims 1 to 4 and 6 to 10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba et al. (U.S. Patent # 6,166,443) in view of David et al. (Japan Patent # 2000-156457).

For example, in claim 1, Inaba et al. **(figure 9)** show a chip scale integrated circuit chip package **21** comprises a die **24** mounted by flip chip interconnection to a first surface of a package substrate **22**, and second level interconnections **28** formed on the first surface of the package substrate. Inaba et al. fail to explicitly show the flip chip interconnection comprises solid state connections of interconnection bumps affixed to the die with interconnection pads on the first surface of the substrate. However, Rolda, Jr. et al. does discloses the structures claimed of the chip, substrate and pads connected. It would be obvious to one of ordinary skill in the art to use solid state connection as a design choice.

David et al. is cited for showing a semiconductor device. Specifically, David et al. (figures 1 to 3) specifically **figure 3** show a chip scale integrated circuit chip package comprising a die **10** mounted by flip chip interconnection to a first surface of a package substrate **14**, wherein the flip chip interconnection comprises solid state connections **(see the abtract's solution section)** of interconnect bumps **18** affixed to the die with interconnect pads **12** on the first surface of the substrate, and second level interconnections **16** formed on the first surface of the package substrate for the purpose

of providing a interconnection of an integrated circuit chip and a board of a multi-chip module.

Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to use David et al.'s solid state connection to modify Inaba et al.'s connection for the purpose of providing a interconnection of an integrated circuit chip and a board of a multi-chip module.

Response

Applicant's arguments filed 12/9/02 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The insertion of Applicant's additional claimed language, for example, "in claim 1" cause for further search and consideration to make this action final.

Applicant's amendment necessitated the new grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL**. See M.P.E.P. § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/686.685,723,777,778,734,737,738,784,786,787,692, 693,698	6/28/02 6/7/03
Other Documentation: foreign patents and literature in 257/686.685,723,777,778,734,737,738,784,786,787,692, 693,698	6/28/02 6/7/03
Electronic data base(s): U.S. Patents EAST	6/28/02 6/7/03

Papers related to this application may be submitted to Technology Center 2800 by facsimile transmission. Papers should be faxed to Technology Center 2800 via the Technology Center 2800 Fax center located in Crystal Plaza 4-5B15. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Technology Center 2800 Fax Center number is (703) 308-7722 or 24. Only Papers related to Technology Center 2800 APPLICATIONS SHOULD BE FAXED to the GROUP 2800 FAX CENTER.

Any inquiry concerning this communication or any earlier communication from the examiner should be directed to ***Examiner Alexander Williams*** whose telephone number is **(703) 308-4863**.

Any inquiry of a general nature or relating to the status of this application should be directed to the ***Technology Center 2800 receptionist*** whose telephone number is **(703) 308-0956**.

6/7/03

Primary Examiner
Alexander O. Williams